8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection :
  HBM EIA/JESD22-A114-A exceeds 2000V
  MM EIA/JESD22-A115-A exceeds 200V

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

The IT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The IT595 is an 8-stage serial shift register with a storage register and 3-stage outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_CP input. The data in each register is transferred to the storage register on a positive-going transition of the ST_CP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7 ') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

GND = 0 V ; T_{amb} = 25°C ; t_r=t_f=6ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			IT595	
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7' SH_CP to Qn $\overline{MR}$ to Q7'	C_L = 50pF ; V_{CC}=4.5V	 13 12 14	 ns ns ns
f_{max}	maximum clock frequency SH_CP and ST_CP		100	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	115	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in PF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs,
   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For IT595 the condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT					OUTPUT		FUNCTION
SH_CP	**ST_CP**	**$\overline{OE}$**	**$\overline{MR}$**	**DS**	**Q7'**	**Qn**	
X	X	L	L	X	L	n.c.	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6'	n.c.	logic high level shifted into shift register stage 0;contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6') appears on the serial output (Q7')
X	↑	L	H	X	n.c.	Qn'	contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6'	Qn'	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   ↑ = LOW-to-HIGH transition;
   Z = high-impedance OFF-stage;
   n.c. = no change;
   X = don't care.

PINNING

PIN	SYMBOL	DESCRIPTION
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0 V)
9	Q7'	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	output enable (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V_{CC}	positive supply voltage

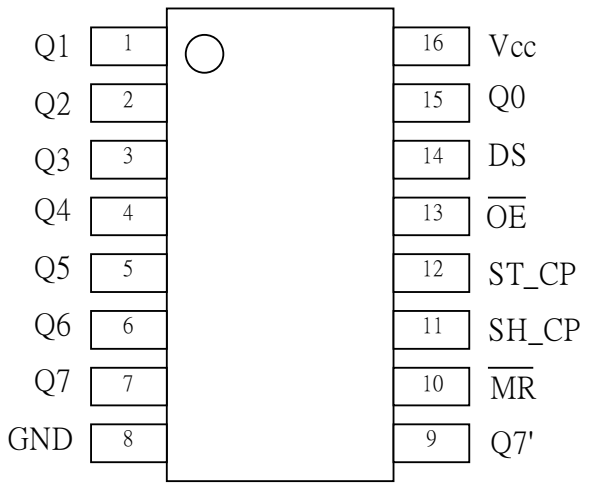


Fig.1 Pin configuration

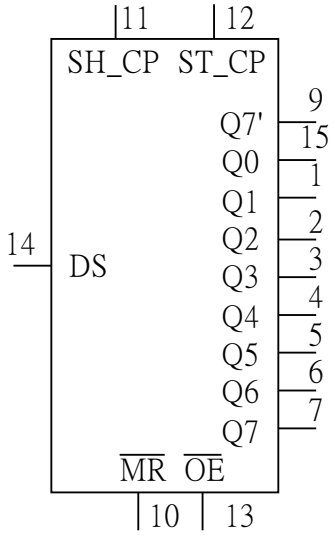


Fig.2 Logic symbol

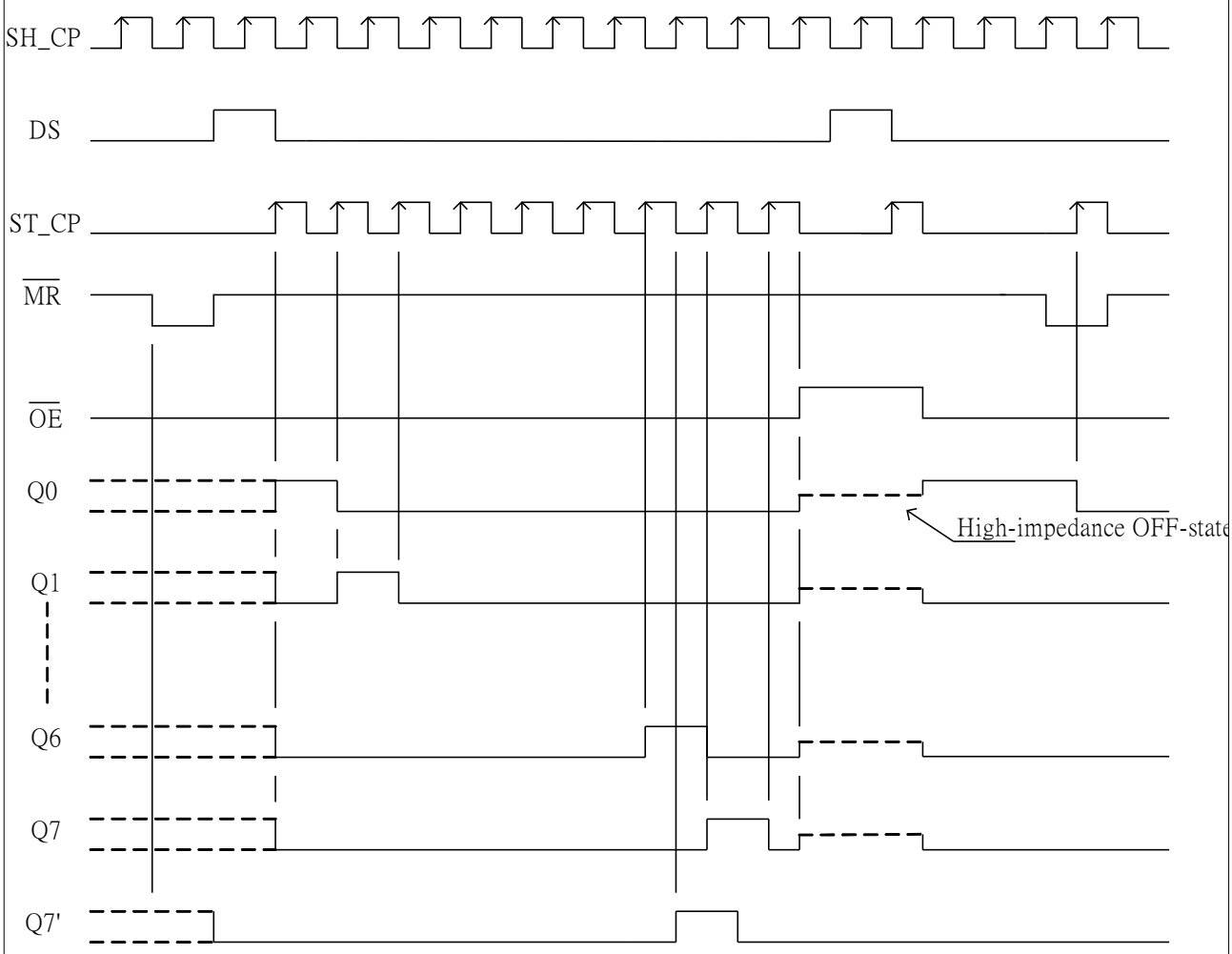


Fig.3 Timing diagram

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	IT595			UNIT
			MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0		VCC	V
V_O	output voltage		0		VCC	V
T_{amb}	ambient temperature		-40		+125	ºC
t_r,t_f	input rise and fall time	V_{CC}=2.0V	-	-	1000	ns
		V_{CC}=4.5V	-	6.0	500	ns
		V_{CC}=6.0V	-	-	400	ns

LIMITED VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are reference to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input diode current	V_I < -0.5 V to V_I > V_{CC} + 0.5V	-	±20	mA
I_{OK}	output diode current	V_I < -0.5 V to V_I > V_{CC} + 0.5V		±20	mA
I_O	output source or sink current	V_O = -0.5 V to V_{CC} + 0.5V Q7' standard output Qn bus driver outputs	 - -	 ±25 ±35	 mA mA
I_{CC} ,I_{GND}	V_{CC} or GND current		-	±70	mA
T_{stg}	storage temperature		-65	+150	ºC
P_{tot}	power dissipation	T_{amb} = -40 to +125ºC; note 1	-	500	mW

DC CHARACTERISTICS

Type IT595
At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

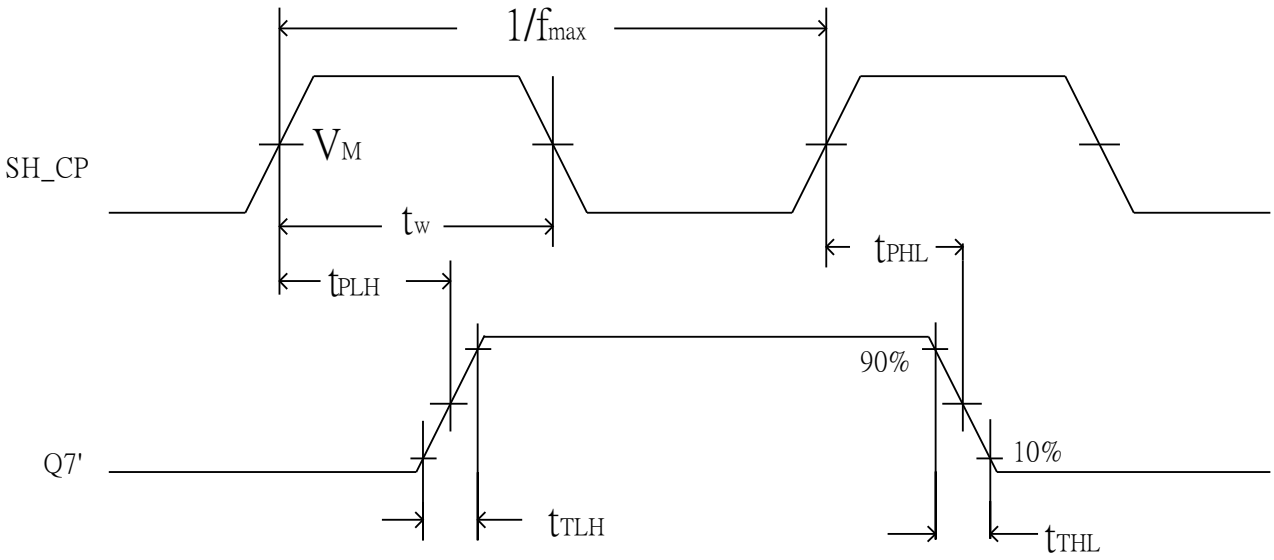
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = -40 to +120^{0}C							
V_{IH}	HIGH-level		2.0	1.5	-	-	V
			4.5	3.15	-	-	V
			6.0	4.2	-	-	V
V_{IL}	LOW-level input voltage		2.0	-	-	0.5	V
			4.5	-	-	1.35	V
			6.0	-	-	2.5	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs I_O=-20µA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	- - -	V V V
		Q7' standard output I_O=-4.12mA I_O=-5.57mA	 4.5 6.0	 - -	 4.12 5.57	 - -	 V V
		Qn bus driver outputs I_O=-4.32 mA I_O=-5.69 mA	 4.5 6.0	 - -	 4.32 5.69	 - -	 V V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs I_O=20µA	2.0 4.5 6.0	- - -	0 0 0	0.1 0.1 0.1	V V V
		Q7' standard output I_O=4.7mA I_O=6.1mA	 4.5 6.0	 - -	 0.33 0.33	 - -	 V V
		Qn bus driver outputs I_O=8 mA I_O=9.3 mA	 4.5 6.0	 - -	 0.33 0.33	 - -	 V V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	-	-	±2	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND	6.0	-	-	±5	µA
I_{CC}	quiescent supply current	V_I = Vcc or GND I_O = 0	6.0	-	-	80	µA

AC CHARACTERISTICS

Family IT595
GND = 0 V ; $t_r = t_f$ = 6ns; C_L = 50pF

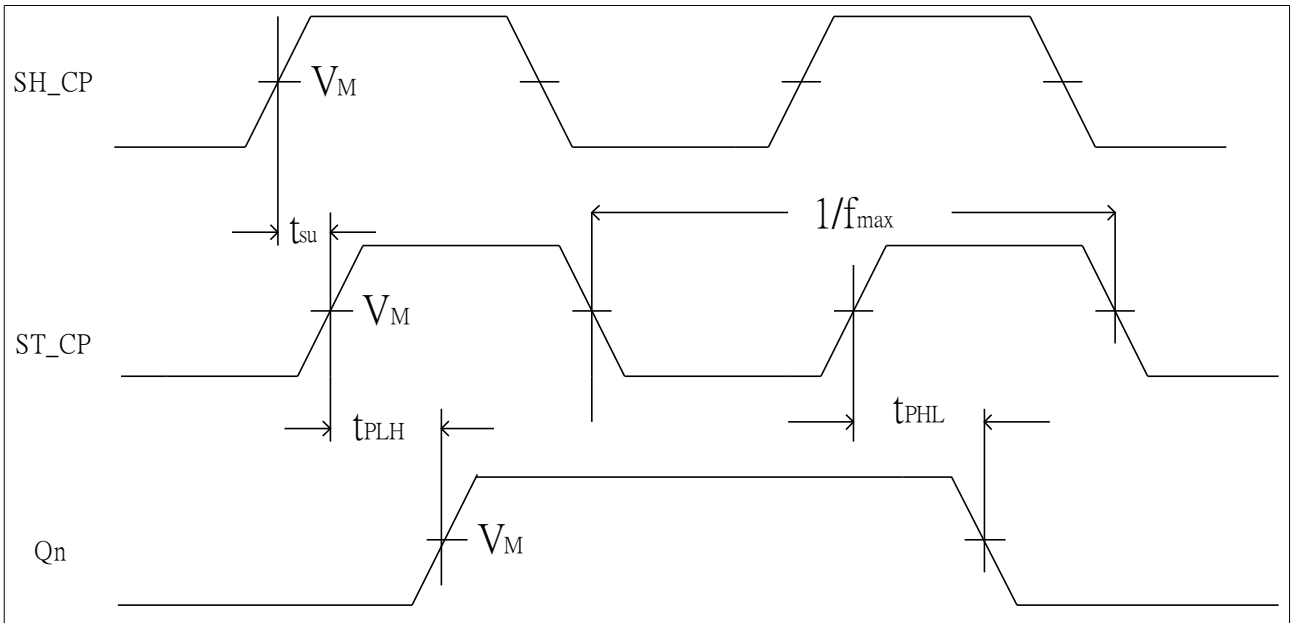
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC}(V)				
T_{amb} = 25 ^{O}C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7'	see Fig.4	2.0	-	24	60	ns
			4.5	-	13	18	ns
			6.0	-	12	16	ns
	propagation delay ST_CP to Qn	see Fig.5	2.0	-	27	52	ns
			4.5	-	12	22	ns
			6.0	-	11	114	ns
t_{PHL}	propagation delay to $\overline{MR}$ Q7'	see Fig.7	2.0	-	32	-	ns
			4.5	-	14	-	ns
			6.0	-	13	-	ns
t_{PZH}/t_{PZL}	3-state output enable time to $\overline{OE}$ Qn	see Fig.8	2.0	-	47	76	ns
			4.5	-	17	24	ns
			6.0	-	14	22	ns
t_{PHZ}/t_{PLZ}	3-state output $\overline{OE}$ disable time to Qn	see Fig.8	2.0	-	40	74	ns
			4.5	-	14	22	ns
			6.0	-	12	20	ns
t_w	shift clock pulse width HIGH or LOW	see Fig.4	2.0	75	17	-	ns
			4.5	15	4	-	ns
			6.0	13	3	-	ns
	storage clock pulse width HIGH or LOW	see Fig.5	2.0	75	17	-	ns
			4.5	15	4	-	ns
			6.0	13	3	-	ns
	master reset pulse width LOW	see Fig.7	2.0	75	17	-	ns
			4.5	15	6		ns
			6.0	13	5	-	ns
t_{su}	set-up time DS to SH_CP	see Fig.6	2.0	50	11	-	ns
			4.5	10	5	-	ns
			6.0	9	5	-	ns
	set-up time SH_CP to ST_CP	see Fig.5	2.0	75	22	-	ns
			4.5	15	8	-	ns
			6.0	14	7	-	ns
t_h	hold time DS to SH_CP	see Fig6	2.0	10	5	-	ns
			4.5	10	5	-	ns
			6.0	10	5	-	ns

AC WAVEFORMS



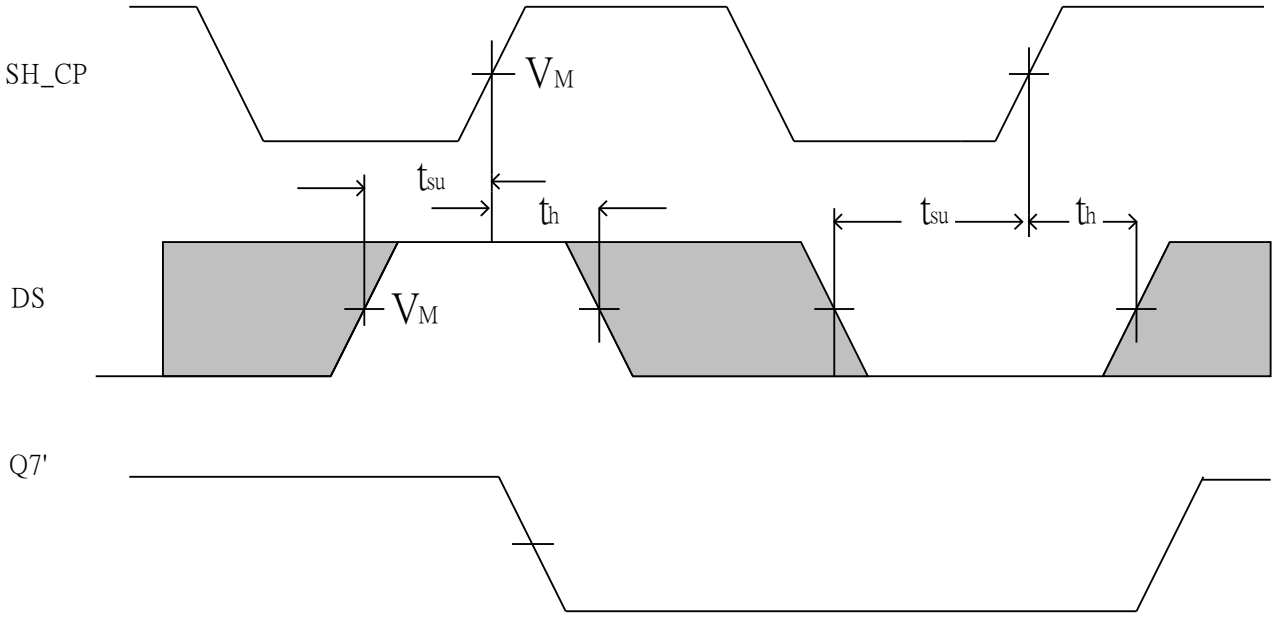
V_M = 50%; V_I = GND to V_{CC}

Fig.4 Waveforms showing the clock (SH_CP) to output (Q7') propagation delays, the shift clock pulse width and maximum shift clock frequency



V_M = 50%; V_I = GND to V_{CC}

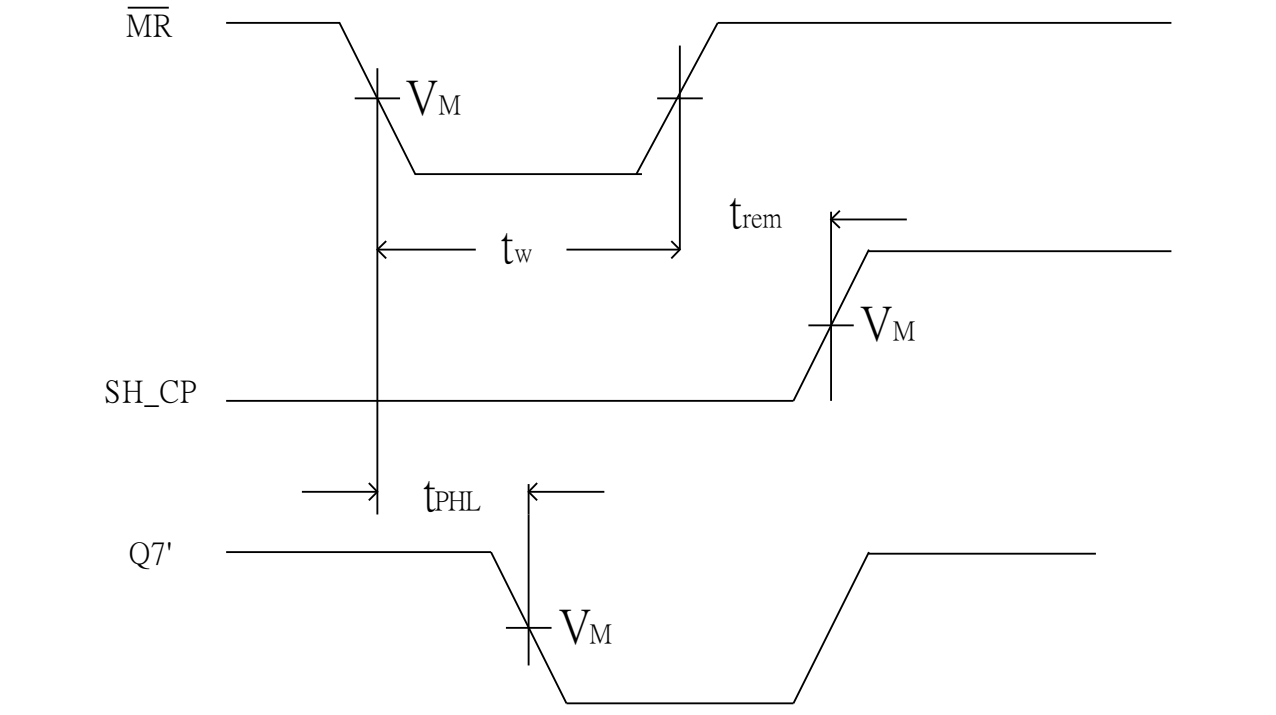
Fig.5 Waveforms showing the storage clock (ST_CP) to output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time



V_M = 50%; V_I = GND to V_{CC}

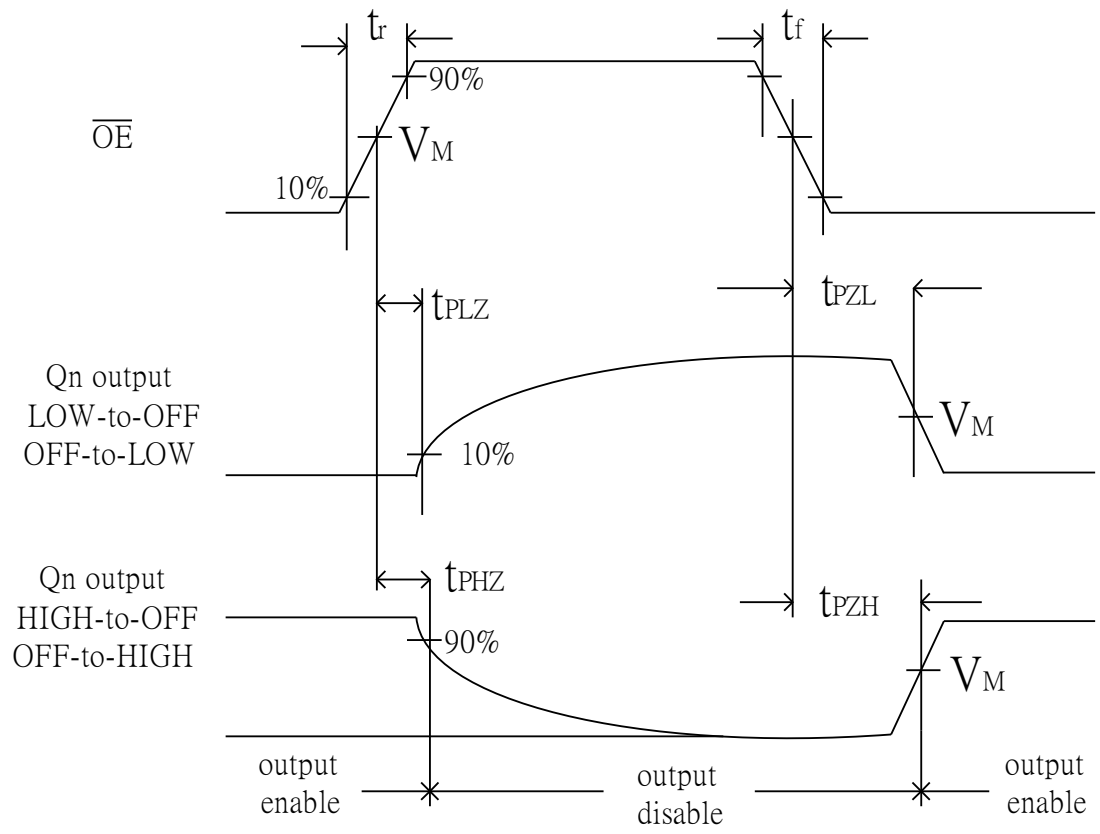
The shaded areas indicate when the input is permitted to change for predictable output performance

Fig.6 Waveforms showing the data set-up and hold times for the DS input



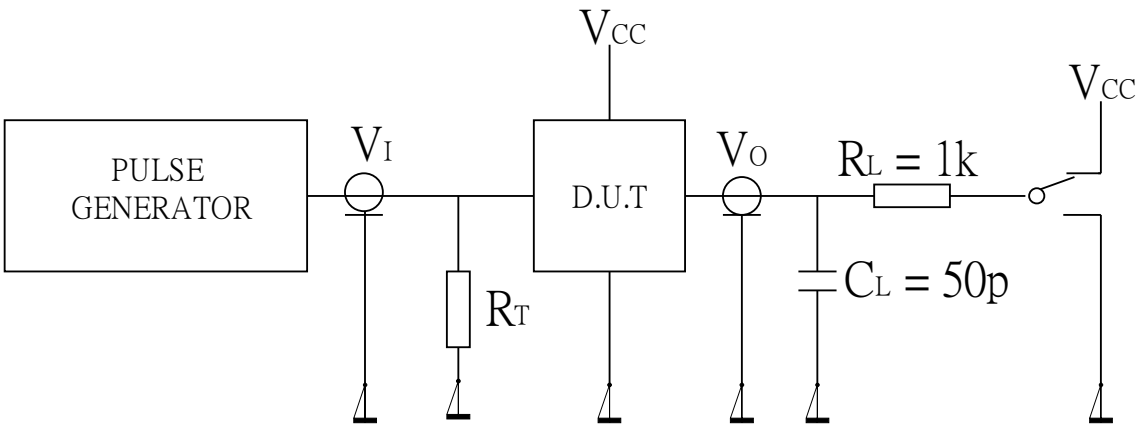
V_M = 50%; V_I = GND to V_{CC}

Fig.7 Waveforms showing the Master Reset ($\overline{MR}$) pulse width, the master reset to output (Q7') propagation delay and the master reset to shift clock (SH_CP) removal time



V_M = 50%; V_I = GND to V_{CC}

Fig. 8 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$



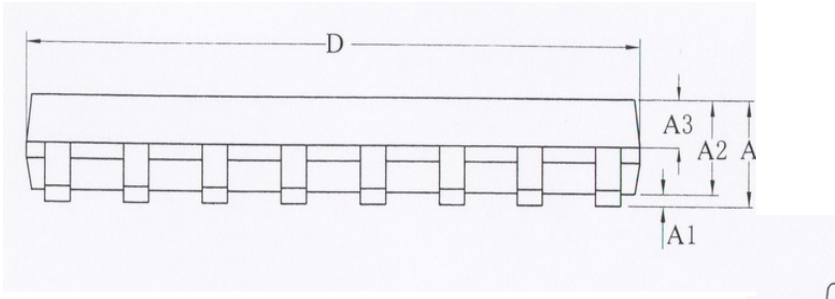
TEST	SWITCH
t_{PLH} / t_{PHL}	open
t_{PLZ} / t_{PZL}	V_{CC}
t_{PHZ} / t_{PZH}	GND

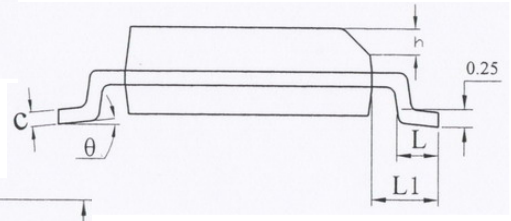
Definitions for test circuit :
R_L = Load resistor
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator

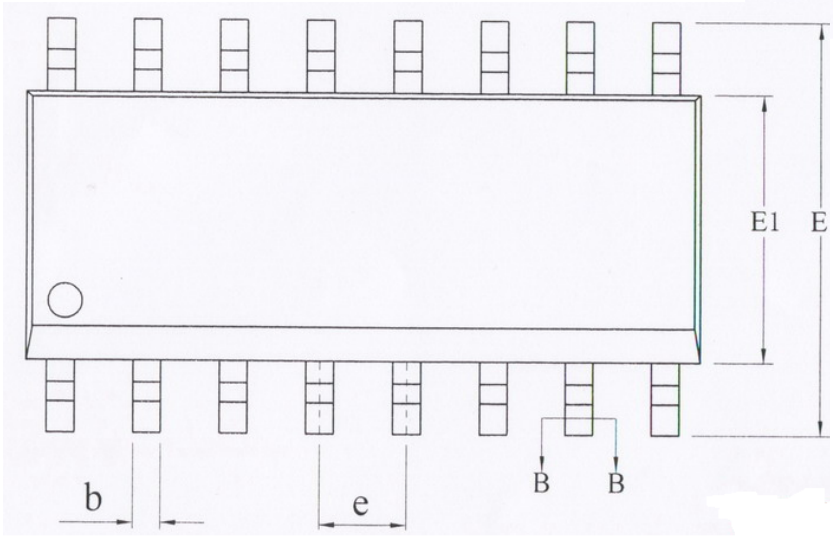
Fig. 9 Test circuit for 3-state outputs

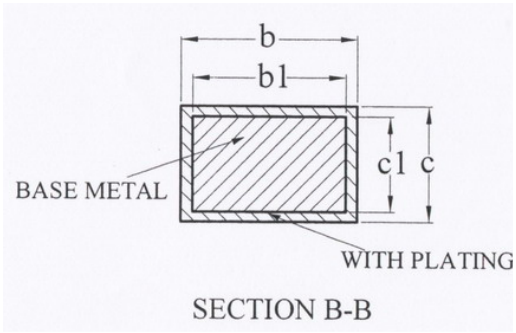
PACKAGE OUTLINES

SOP16L









SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	75*75		
	90*110	95*110	
	90*180	95*180	